REMARKS

In the Office Action, the Examiner rejected Claims 2-19, which were all of the then pending claims, over the prior art, principally U.S. Patent 6,845,432 (Maiyuran, et al.). In particular, Claims 2-18 were rejected under 35 U.S.C. 103 as being unpatentable over Maiyuran, et al. in view of U.S. Patent 6,421,809 (Wuytack, et al.), and Claim 19 was rejected under 35 U.S.C. 102 as being fully anticipated by Maiyuran, et al.

Independent Claims 2, 10, 16 and 19 are being amended to better define the subject matters of these claims. Claims 5, 8, 13 and 14 are being cancelled to reduce the number of issues in this case, and Claim 6 is being amended to be dependent from Claim 2 instead of the now cancelled Claim 5. Claim 20, which is dependent from Claim 10, is being added to describe preferred features of the invention.

For the reasons discussed below, Claims 2-4, 6, 7, 9-12 and 15-20 patentably distinguish over the prior art and are allowable. The Examiner is thus asked to reconsider and to withdraw the rejection of Claims 2-4, 6, 7, 9-12 and 15-18 under 35 U.S.C. 103 and the rejection of Claim 19 under 35 U.S.C. 102, and to allow Claims 2-4, 6, 7, 9-12 and 15-20.

Generally, Claims 2-4, 6, 7, 9-12 and 15-20 patentably distinguish over the prior art and are allowable because the prior art references do not disclose or suggest maintaining coherency of data in the cache, as described in independent Claims 2, 10, 16 and 19. More specifically, the prior art references do not show or suggest ensuring that, as selected areas or sections of the cache are powered off, copies of all data elements in the cache exist in an area or in sections of the cache not powered off.

To best understand this difference and its significance, it may be helpful to review briefly this invention and the prior art.

The present invention, generally, relates to dynamically controlling caches size. As discussed in the present application, currently, the cache size and cache power consumption remain constant during microprocessor usage. For example, even during low power operation, the full DC portion of the power consumption is still dissipated, serving no purpose.

The present invention addresses this issue. In particular, this invention provides a method and apparatus for powering down sections of a microprocessor cache to minimize power consumption, and the instant invention does this while not impacting cache operation when high performance is required.

Generally, the present invention does this by providing a power saving cache comprising circuitry to dynamically reduce the logical size of the cache in order to save power, and means for determining an optimal cache size for balancing power and performance. More specifically, in the operation of this cache, the logical size of the cache is reduced by powering off selected areas of the cache. Also, the cache includes means for maintaining coherency of the cache, as the cache size is reduced, by ensuring that copies of all data elements in the cache exist in an area of the cache not powered off.

The references of record to not disclose or suggest maintaining data coherency in this way.

For example, Maiyuran, et al. describes a low power cache architecture comprised of a set of modules. To reduce power consumption, each module may be powered down independently of the other modules. Maiyuran, et al, however, does not disclose or suggest maintaining data coherency in the above-discussed manner.

In the Office Action, the Examiner cited column 2, lines 16-17 of Maiyuran, et al. for its disclosure of cache coherency state information. This portion of Maiyuran, et al. describes

that a state field S is used to indicate the state of cache coherency. This very different from what the present invention does. In particular, indicating the state of cache coherency (as is done in Maiyuran, et al.) is very different from maintaining cache coherency (as is done in the present invention).

Independent Claims 2, 10, 16 and 19 are being amended to emphasize the above-discussed difference between this invention and the prior art. Specifically, Claim 1, which is directed to a power saving cache, is being amended to describe the feature that selected areas of the cache are powered off, and to describe means for maintaining coherency of data in the cache, as the size of the cache is altered, by ensuring that copies of all date elements in the cache exist in an area of the cache not powered off.

Claims 10 and 16 are method claims directed to a method of operating a power saving cache, and both of these claims describe method features analogous to the apparatus features discussed above in connection with Claim 2. Claim 19, similarly, is a method claim that also defines a method of operating a power saving cache, and Claim 19 is being amended herein to positively set forth the step of ensuring that copies of all data elements in the cache exist in sections of the cache not powered off.

The above-discussed feature of the present invention is of utility because it allows the cache – and the processor using the cache – not only to reduce power consumption, but also to do this in a way that does not impact cache operation when high performance is required.

The other references of record have been reviewed, and these other references, whether considered individually or in combination, also do not disclose or suggest this feature of the instant invention.

For instance, Wuytack, et al. was cited for its disclosure of a procedure for determining an optimal memory size. This reference relates to designing a memory organization, and clearly Wuytack, et al. does not describe or address procedures for maintaining cache coherency as sections or areas of the cache are powered down.

Because of the above-discussed differences between Claims 2, 10, 16 and 19 and the prior art, and because of the advantages associated with those differences, these claims patentably distinguish over the prior art and are allowable. Claims 3, 4, 6, 7 and 9 are dependent from, and are allowable with Claim 1; and Claims 11, 12, 15 and 20 are dependent from Claim 10 and are allowable therewith. Likewise, Claims 17 and 18 are dependent from Claim 16 and are allowable therewith. Accordingly, the Examiner is respectfully requested to reconsider and to withdraw the rejection of Claims 2-4, 6, 7, 9-12 and 15-18 under 35 U.S.C. 103 and the rejection of Claim 19 under 35 U.S.C. 102, and to allow claims 2-4, 6, 7, 9-12 and 15-20.

Every effort has been made to place this application in condition for allowance, a notice of which is requested. If the Examiner believes that a telephone conference with Applicants' Attorneys would be advantageous to the disposition of this case, the Examiner is asked to telephone the undersigned.

Respectfully submitted,

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